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Proposed structure of fault current limiter with power quality improvement

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Abstract— This paper presents controlling the magnitude of fault current by using non super conducting fault current limiter with the help of controlled rectifier. Non superconducting fault current limiter consists of a rectifier and D. C reactor. The diode rectifiers are uncontrollable, to make it as a controllable by replacing the thyristor in place of diode. By providing the suitable gate triggering to the thyristor circuit we can control the magnitude of current in DC reactor. By reduce the magnitude of fault current in a power system, which improve the voltage profile at faulted phase. The proposed NSFCL was simulated and studied with the help of MAT-LAB.

Index Terms— fault current limiter, fault currents, non super conductor, and thyristor controlled rectifier

1 INTRODUCTION

Power quality problems are becoming more and more important for utilities due to growing number of sensitive loads. Short circuit results the large amount of current flow through the distribution network. The large fault currents flow may damage the series equipment, such as circuit breaker and other system components. The Fault current causes the voltage drop of a particular network. As a result, some industrial facilities experience production outage that results in economic losses. Therefore, utilities are currently exploring mitigation techniques that eliminate large fault current, increase the reliability of the power supply and improve the reliability and the system power quality. The most common ways to limit fault currents are the costly replacement of substation equipments or imposition of changes in the configuration splitting power system that may lead to decreased operational flexibility and lower reliability.

A novel idea is to use Fault Current Limiters to reduce the fault current to lower, acceptable level so that the existing switchgear can still be used to protect the power grid. An ideal FCL should have the following characteristics

a) Zero resistance/impedance at normal operation;
b) No power loss in normal operation and fault cases;
c) Large impedance in fault conditions;
d) Quick appearance of impedance when fault occurs;
e) Fast recovery after fault removal;
f) Reliable current limitation at defined fault current;
g) Good reliability;
h) Low cost.

Different configurations such as Is - limiters, solid state fault current limiters and superconducting fault current limiters were proposed in previous papers [6] [7] [8]. The SFCL structure offers a good way to control the fault current levels in distribution networks due to natural low losses in superconductors during the normal operation. Unfortunately, because of high technology and cost of superconductors, these devices are not commercially available. Therefore, replacing the superconducting coil with nonsuperconducting coil in FCL makes it simpler and much cheaper.

This paper proposes magnitude of fault current controlled by using thyristor circuit of a non super conducting fault limiter. And also improves the voltage profile in a network.The circuit operation in normal and fault conditions are simulated and experienced.

2 CIRCUIT OPERATION

The circuit consists of a three phase transformer is connected to a thyristor circuit at source side. By providing the gate pulse to the thyristors to control the magnitude of fault current. And another three phase transformer is connected to a diode bridge rectifier at load side. The diode bridge rectifier is connected to a parallel connection of a discharging resistor and a thyristor switch and is connected in series with the D.C reactor is shown in figure.1.

In normal operation that is without fault condition semiconductor switch is turn on. And resultant current flows through the diode rectifier and discharging resistor. And normal current flows to the thyristor circuit. By increasing the inductance value decreases the ripple of D.C current. During the fault condition, the switch is turn on that is when fault take place at load side then it results the D.C reactor current increases linearly. If the fault is present for long time the current through the D.C reactor will continue to increase. And results the source voltage drop take place. There is a control circuit present by using that we can control the magnitude of fault current in case of diode rectifier circuit in previous paper[1]. That control circuit consists of a discharging resistor and a switch along with resistor. When a fault take place the switch can be turn on and fault current flows to the parallel resistor and it results the voltage drop take place at source side. In order to reduce the magnitude of fault current the switch can be turn-off and the fault current flows through the discharging resistor. It results there is a reduction of magnitude of fault current and improves the voltage profile at source side.

In this paper without using the control circuit we can control the fault current within prescribed below limits. That is in normal operation switch is turn on and normal current flows through the D.C reactor. In case of fault switch is

turn on then the D.C reactor current increases. To control the magnitude of fault current by varying the duty cycle of thyristor circuit to reduce the magnitude of fault current in D.C reactor without using control circuit. Therefore it improves the voltage profile at source side. Due to controlling the D.C reactor current of proposed NSFCL, it is possible to reduce the current rating of inductance and cancelling out the super conducting cooling system. The compensating voltage provided by rectifier is

$$V_c=2v_{DF}+v_{sw}+r_dL_d \quad (1)$$

3 MATHEMATICAL ANALYSIS

The circuit has two modes of operations after fault as follows: A) The fault current has not reached to specified current level (I_d)

B) The fault current is reached to specified current level (I_d). Figure.2 shows the line and DC reactor currents during first mode from t_0 to t_4. In order to simplify the analysis, the

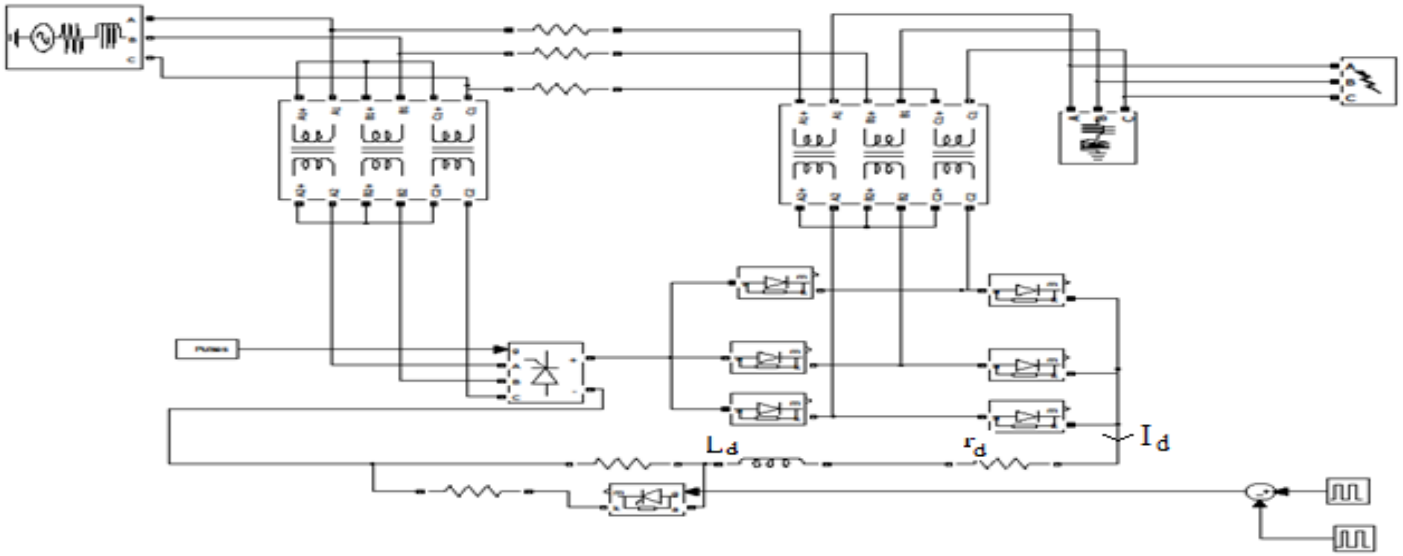


Figure.1 circuit diagram

Turns ratio of an isolation transformer is considered equal to one. In this figure, t_0 and I_c stand for short circuit instant and specified level for line current, respectively. In this mode, the semiconductor switch is closed and we have two sub-modes as follows

a) Charging mode (between t_0 and t_1 and between t_2 and t_3 in Figure. 2);

b) Discharging mode (between t_1 and t_2 and between t_3 and t_4 in Figure. 2).

During charging mode, the DC reactor current is equal to the line current, and we have the following equation is

$$V\sin\omega t+v_c=ri_L(t)+L[di_L(t)/dt]+2v_{DF} \quad (2)$$

Where v_c is the compensation voltage and v_{DF} is the voltage drop across the diodes.

So, the utility and DC reactor current equations can be derived as shown. This equation 2 can be solved by using the steady state and transient analysis

$$i(t)=e^{-(r/L)(t-t_0)}[i_0-(v/z)\sin(\omega t_0-\varphi)+(2v_{DF}-v_c)/r]+(v/z)\sin(\omega t-\varphi)-[(2v_{DF}-v_c)/r] \quad (3)$$

$$\text{Where } r = r_s + r_f + r_d$$
$$L = L_s + L_f + L_d$$
$$i_L(t) = i_d(t) = i(t),\ z=\sqrt{r^2+(L\omega)^2},\ i_0 = i(t_0)$$

Where r_f and L_f stand for resistance and inductance of fault impedance, respectively.

During discharging mode, the DC reactor current is more than line current, and the DC reactor current freewheels through the diodes of the isolation transformer and voltage transformer rectifiers. In this mode, we have

$$V\sin\omega t=ri_L(t)+L[di_L(t)/dt] \quad (4)$$

Where

$$r = r_s + r_f$$
$$L = L_s + L_f$$

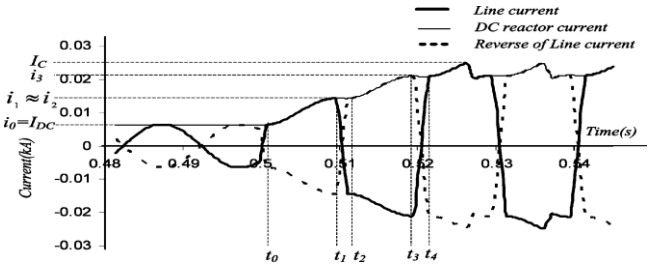


Figure.2 Line and dc reactor current after fault and before semiconductor switch operation

Now line current is

$$i(t) = e^{-(r/L)(t-t_1)}[i_1-(v/z)\sin(\omega t_1-\varphi)+(2v_{DF}-v_c)/r] + (v/z)\sin(\omega t-\varphi) \quad (5)$$
$$z=\sqrt{r^2+(L\omega)^2},\ i_1 = i(t_1),\varphi=\tan^{-1}(L\omega)/r$$

In addition, it is possible to write the following equation in fault condition and discharging mode too

$$L_d(di_d/dt)+r_d i_d(t)+2v_{DF}-v_c=0 \quad (6)$$

This equation results in the dc reactor current formula given as

$$i(t)=e^{-(r_d/L_d)(t-t_1)}[i_1+(2v_{DF}-v_c)/r]-(2v_{DF}-v_c)/r) \quad (7)$$

After t_2, we have another charging mode from t_2 to t_3 and discharging mode from t_3 to t_4.

After t_4, another charging mode begins but the line current reaches to specified level (I_c) at t_5 , and it results in turn-off of the semiconductor switch by the control circuit. Now, the discharging resistor is inserted in series with the dc reactor. Figure.3 shows the line and dc reactor current in this mode. From t_5 to t_6, the line current and dc reactor current decrease, and we have the following equation

$$V\sin\omega t+v_c=ri_L(t)+L[di_L(t)/dt]+2v_{DF} \quad (8)$$

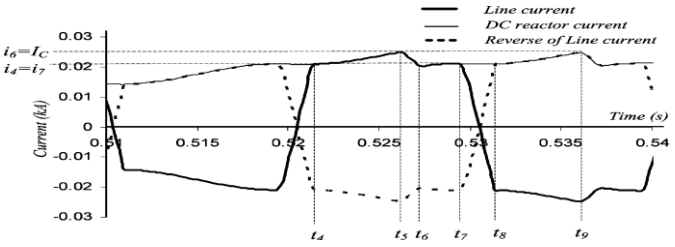


Figure.3 Line and dc reactor current after fault and semi conductor switch Operation

$$i(t) = e^{-(r/L)(t-t_5)}[i_1-(v/z)\sin(\omega t_5-\varphi)+2v_{DF}/r] + (v/z)\sin(\omega t-\varphi)-2v_{DF}/r \quad (9)$$

Where

$r = r_s+r_f+r_d+r_p$

$L = L_s+L_f+L_d$

$i_L(t) = i_d(t) = i(t)$

$z=\sqrt{r^2+(L\omega)^2}$, $i_5 = i(t_5)$, $\varphi=\tan^{-1}(L\omega)/r$

The time interval between t_5 and t_6 is considered as small percentage of power frequency period. At t_6 the semiconductor switch turns on by the control circuit, and we have again charging mode until t_7. Fromt_7 discharging mode begins and it continues until t_8. From t_8, another charging mode begins and it continuous until t_9, where semiconductor switch turns off to insert the discharging resistor in series with the dc reactor. The circuit will have the same periodic operation from t_5 to t_9 until clearance of fault

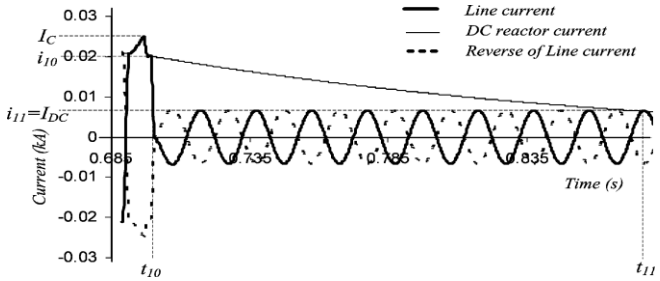
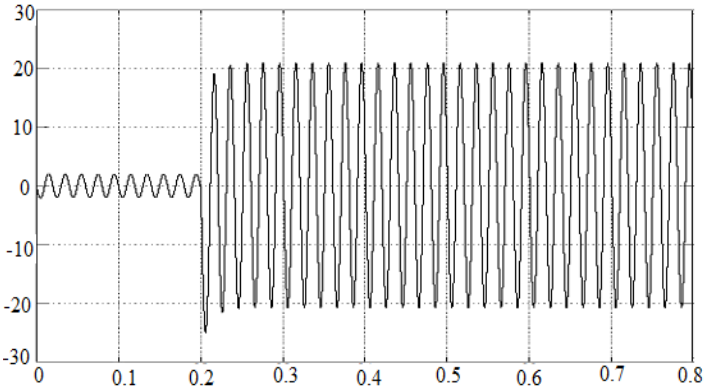


Figure.4 Line and DC reactor current after fault

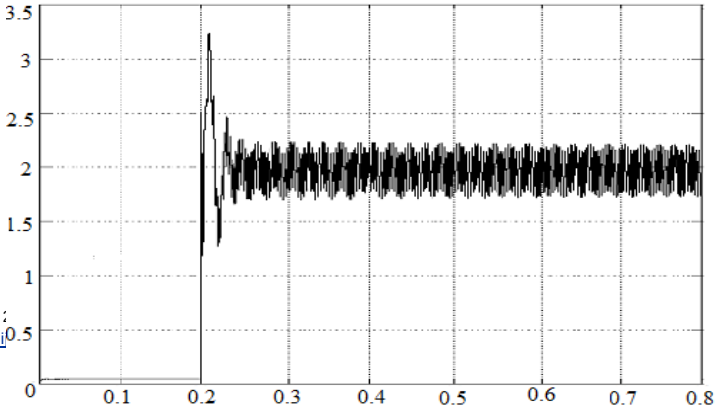
Figure.4 shows the line current and DC reactor current after clearance of fault at t_{10}. During this mode, the DC reactor current decreases because of its discharging resistor r_d, and forward voltage drop on diodes. Clearly, by using the superconducting coil, its current also decreases during the discharging mode, but at a slower rate compared with non-superconducting DC reactor. Fig.4 shows that the DC reactor current discharges to its pre-fault value that is equal to maximum of line current after some milliseconds. In this way, the fault current limiter will be ready to limit the next possible fault without any additional power or control circuit.

4 SIMULATION RESULTS

The power circuit topology is shown in figure.1 is used to simulation. The simulation results are obtained NSFCL operation performance of a thyristor circuit at a fault condition, where a three phase to ground fault occurs at load side. The neutral of source grounded. The various operation performances are carried out as follows.The below figure.5 shows the magnitude of fault line current, figure.6 shows the DC reactor current and figure.7 shows the source voltage drop of a distribution network. By using the thyristor circuit of applying the suitable duty cycle without turn off the switch then the reduced magnitude of fault line current is shown in figure.8, reduced magnitude of DC reactor current is shown in figure.9 and improved source voltage profile obtained shown in figure.10. The enlarged



DC reactor current during the fault shown in figure.11 and DC reactor current during the transient fault were shown



in figure.12.

Figure.5 magnitude of fault current

Figure.6 dc reactor current during the fault

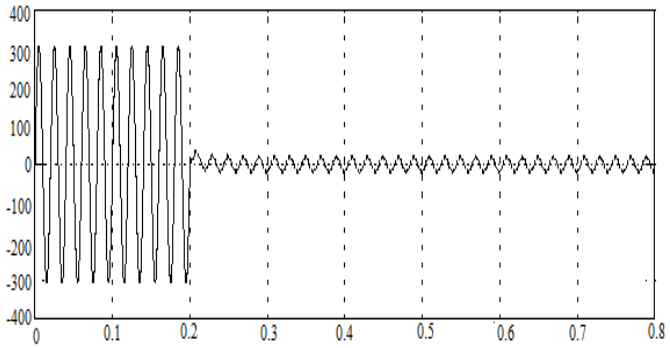


Figure.7 voltage drop during fault

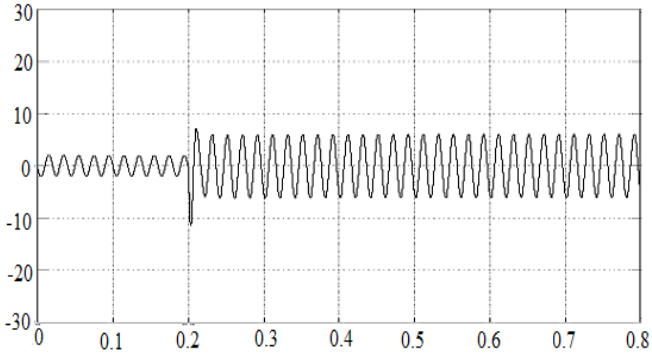


Figure.8 Reduced fault current

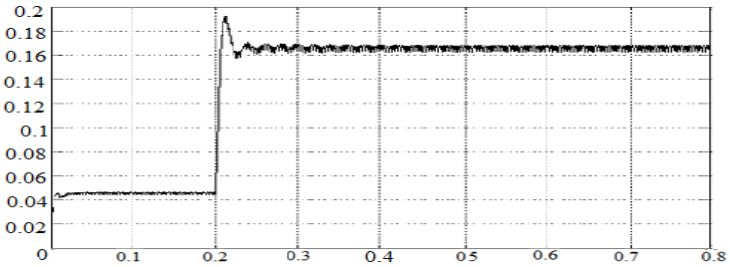


Figure.9 Reduced of dc reactor current

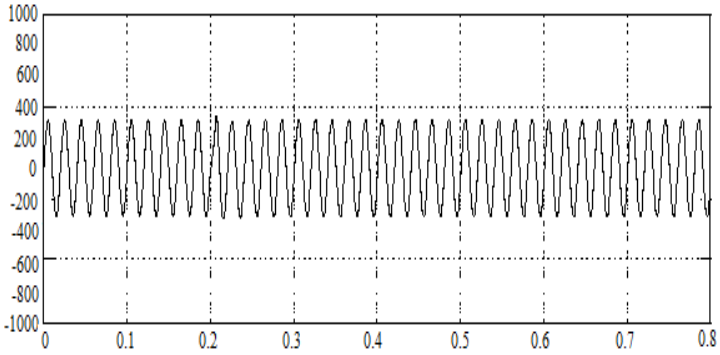
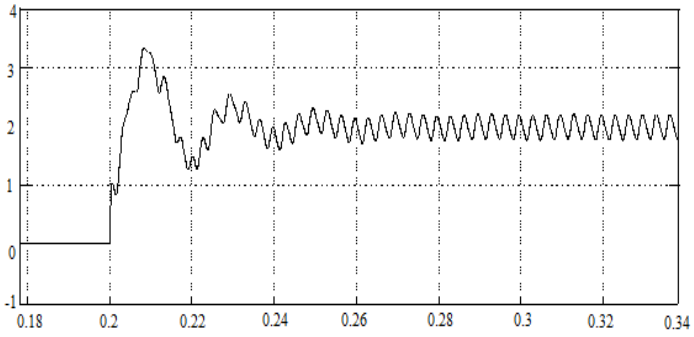


Figure.10 improvement of voltage profile

Figure.11 Enlarged DC reactor current during the fault

Figure.12 dc reactor current during transient faults



4.1 PARAMETERS OF SIMULATION

Symbol	Content	Value
V_s	Source voltage	380V
r_s	Source	1Ω
F	Power frequency	50HZ
V_{DF}	Voltage drop across rectifier diodes	2V
V_{SW}	Voltage drop across semi conductor switch	2V
r_d	DC reactor resistance	0.2Ω
L_d	DC reactor inductance	0.2H
r_p	Discharging resistance	100Ω
r_{Load}	Load resistance	50Ω
L_{Load}	Load inductance	100Ω
r_F	Fault resistance	0.01Ω
L_S	Source inductance	0.01H
Z_{Line}	Line impedance	6Ω

5 CONCLUSION

The three phase to ground fault is most severe fault in any power system. Whenever it happens to the system there is a severe dip in the voltage. This is one of the power quality problems. To mitigate the above problem we need to minimize the fault current. For which in this paper proposed fault current limiter minimizes the fault current and improves the voltage profile which is observed from the simulation result.

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